

GIGABYTE GA-8IG1000 Pro-G Schematics

Revision 3.1

SHEET

TITLE

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3,4 CHANNEL B
13	DDR TERMINATION
14	AGP 8X SLOT
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	DUAL FWH
19	ICS952635 CLOCK GENERATOR
20	PCI SLOT1/SLOT2
21	PCI SLOT3/SLOT4/RESET BUFFER
22	PCI SLOT5/SLOT6

23	AC '97 CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712/IR_CIR/SCR/S_IRQ
26	COMA/VGA_COMB/LPT
27	IDE1/IDE2/FDD
28	FAN/HW MONITOR
29	KB_MS/GAME/FUSEVCC
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31	R_USB/F_USB1/F_USB2
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33	VCORE POWER
34	ATX/ATX_12V/FAN1655M
35	MARVELL 88E8001
36	TI TSB43AB23(1394)
37	PCI ROUNTIONG
38	GPIO PIN LIST

PROCESS: C		COMPONENT SIDE (0.5 oz. Copper)	
		VCC SIDE (1 oz. Copper)	
		GND SIDE (1 oz. Copper)	
		SOLDER SIDE (0.5 oz. Copper)	
GIGABYTE CORP.			
Title: COVER SHEET			
Size: Custom	Document Number: GA-8IG1000 Pro-G		Rev: 3.1
Date:	Sheet 1 of 39		

Component history

Date	Change	Item	Reason
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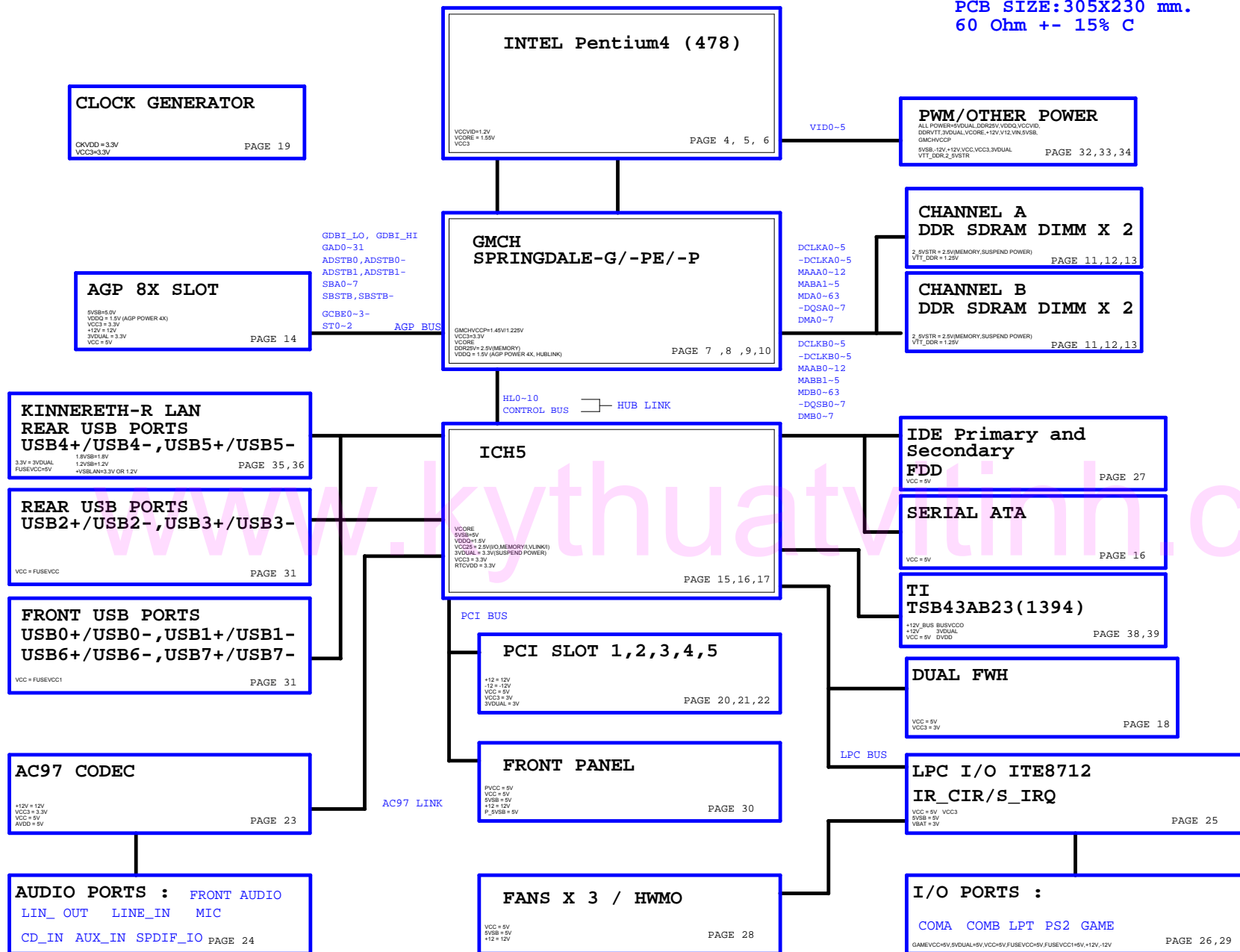
Circuit or PCB layout history

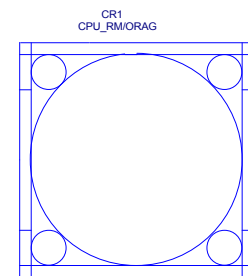
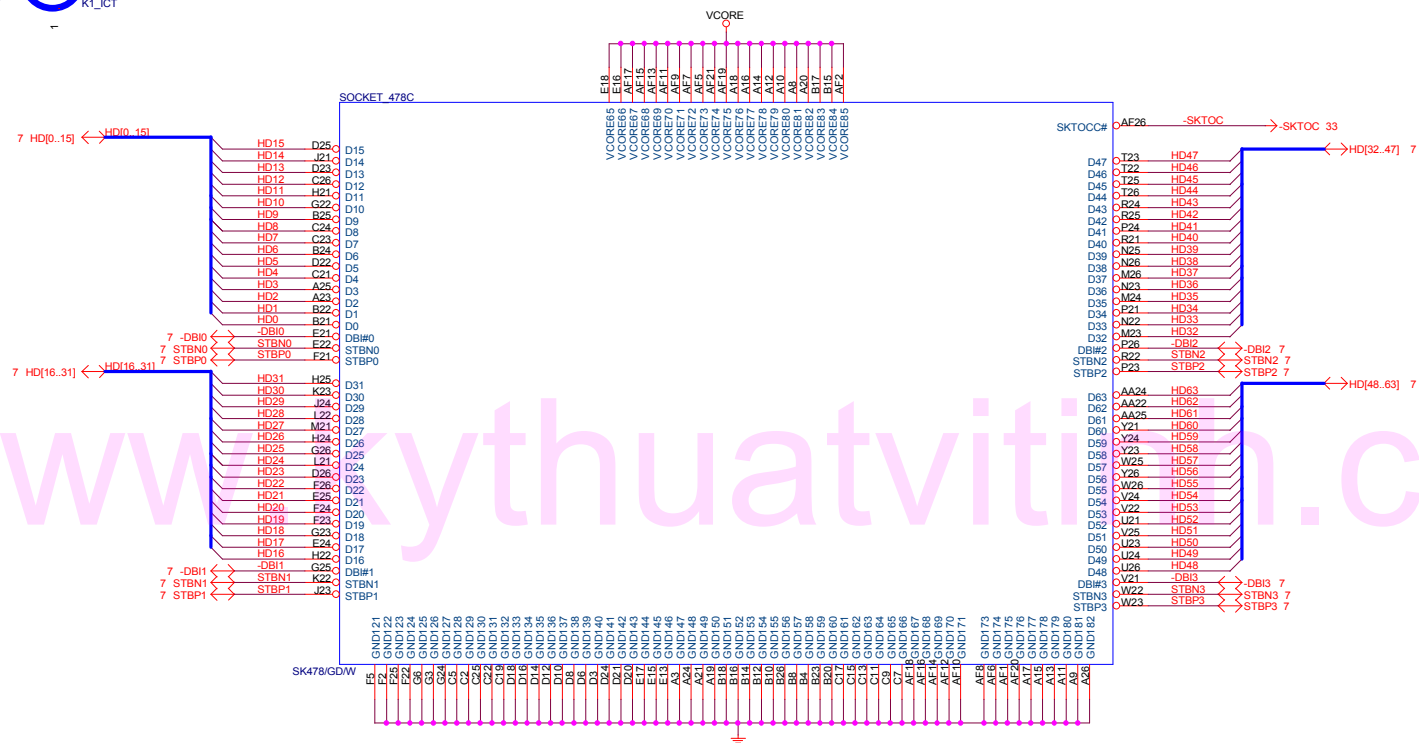
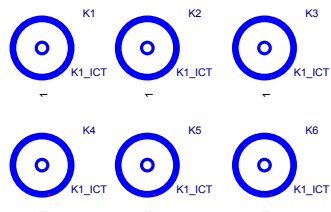
Date	Change Item	Reason
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Title BOM & PCB MODIFY HISTORY			
Size Custom	Document Number GA-8IG1000 Pro-G		Rev 3.1
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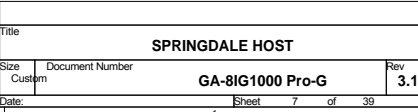
BLOCK DIAGRAM

PCB SIZE:305X230 mm.
60 Ohm +- 15% C



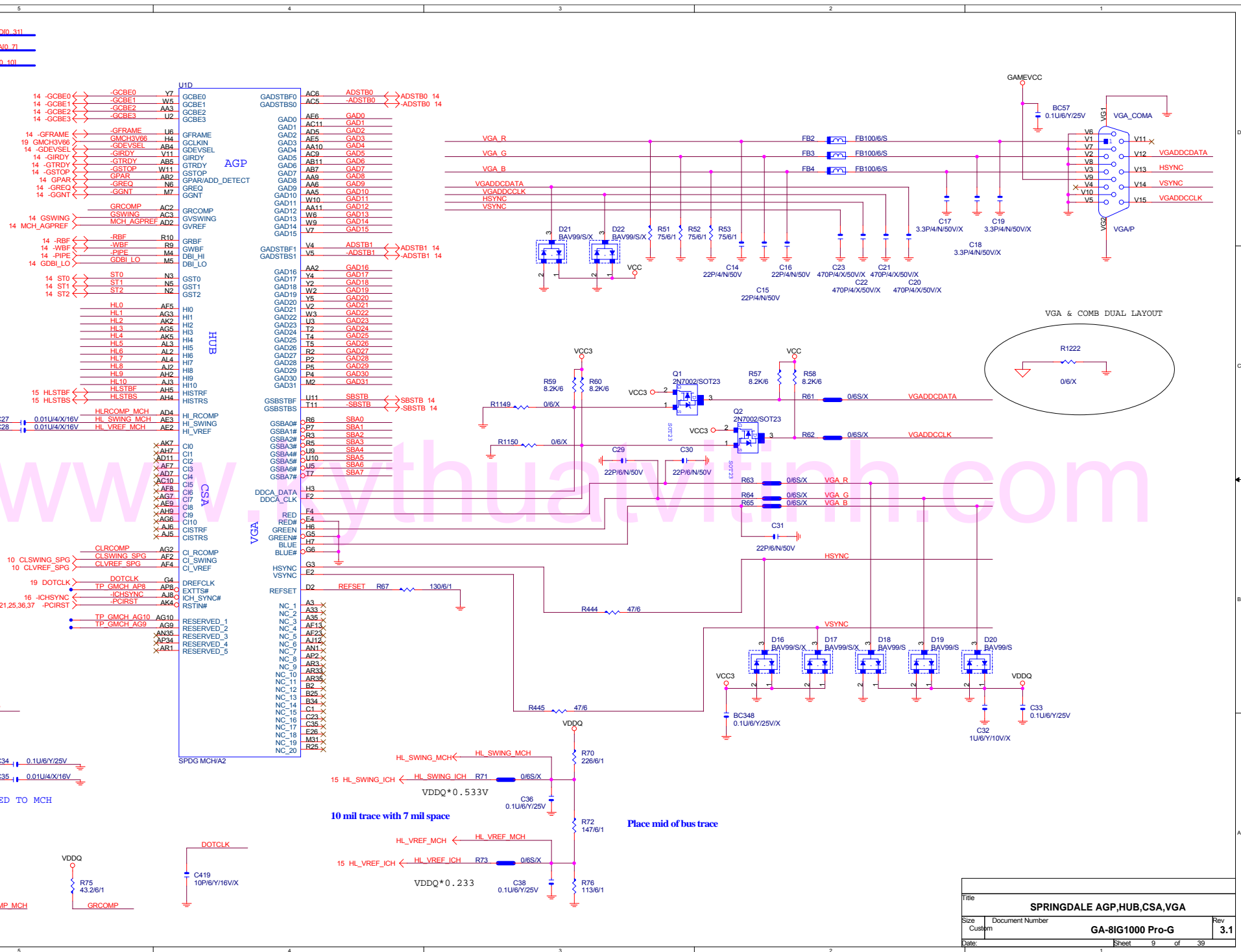


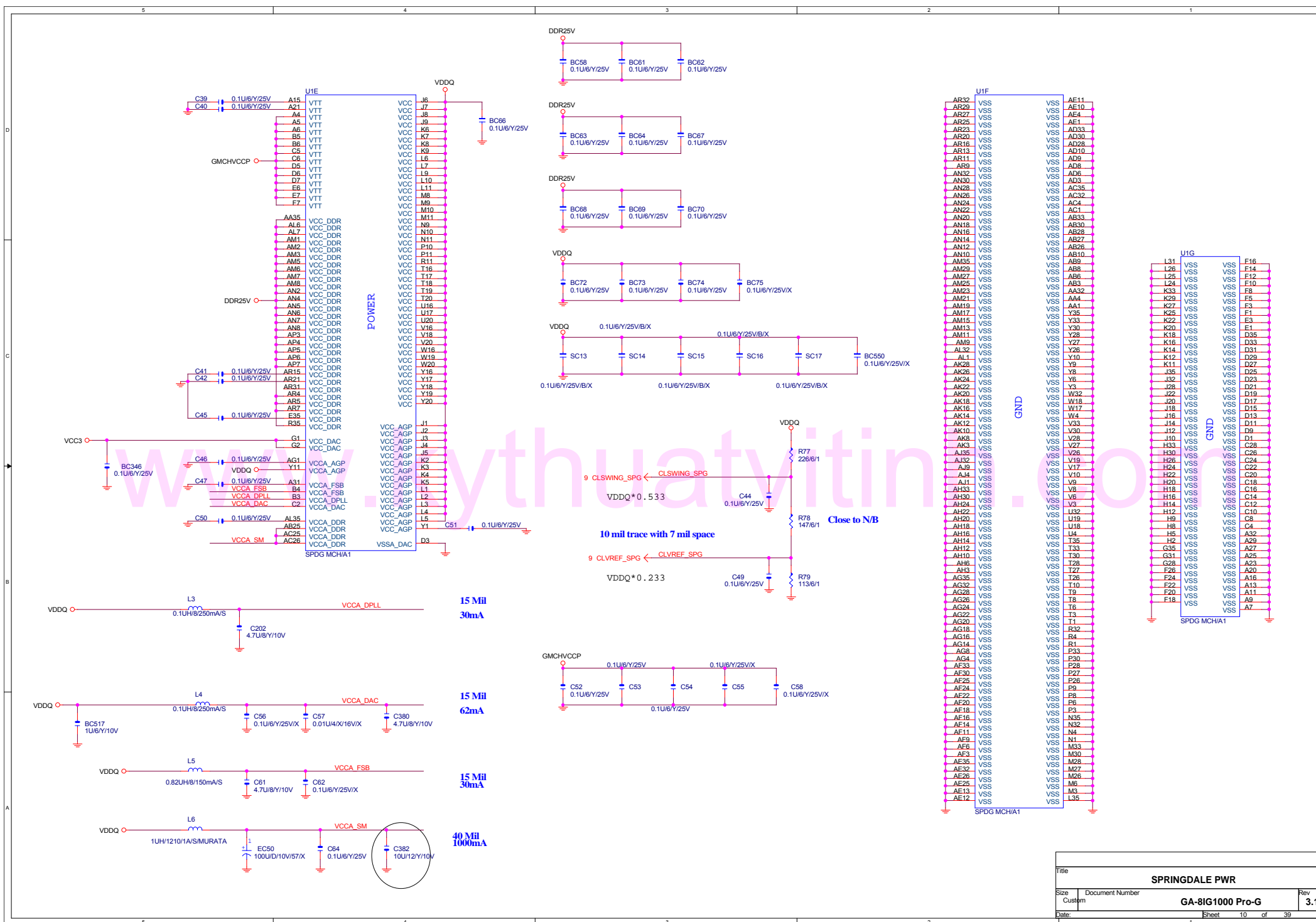
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P4 478C			
Size	Document Number	Rev	
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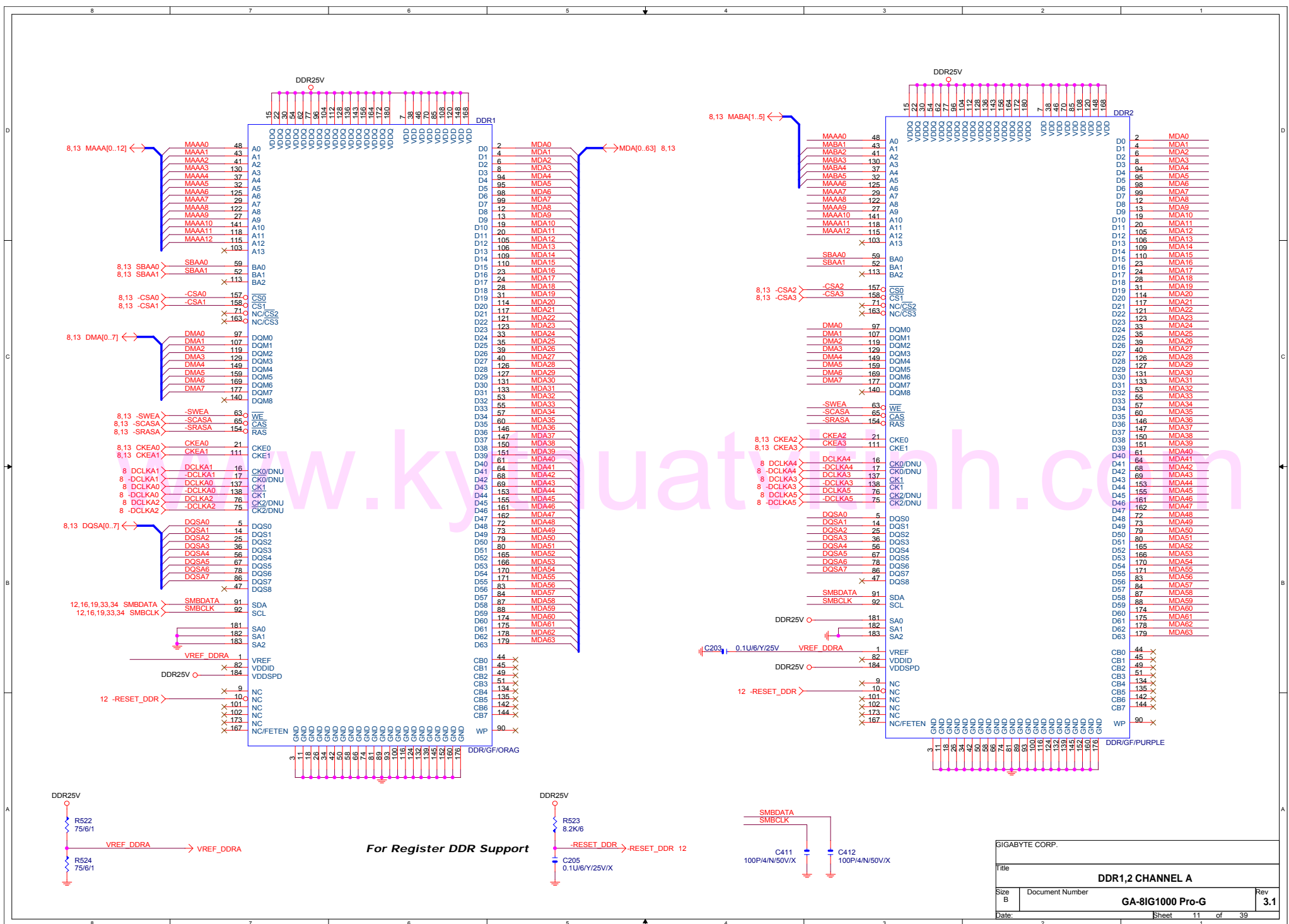


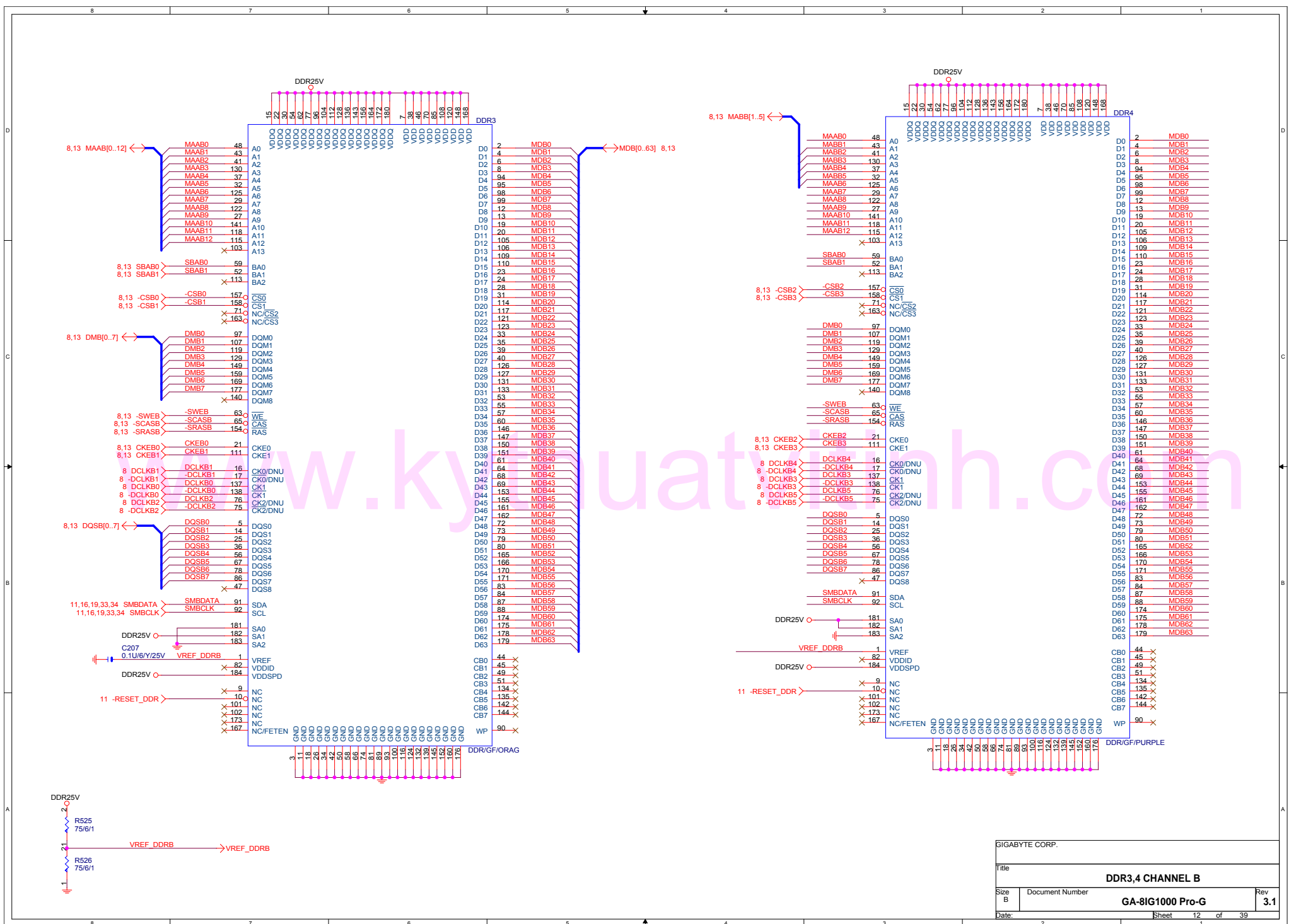
DDR 400 1-2-3-4 CPC DISABLE
DDR 333 SIGNAL 1 CPC ENABLE
2 CPC DISABLE
DUAL 2 CPC ENABLE
DUAL 4 CPC DISABLE



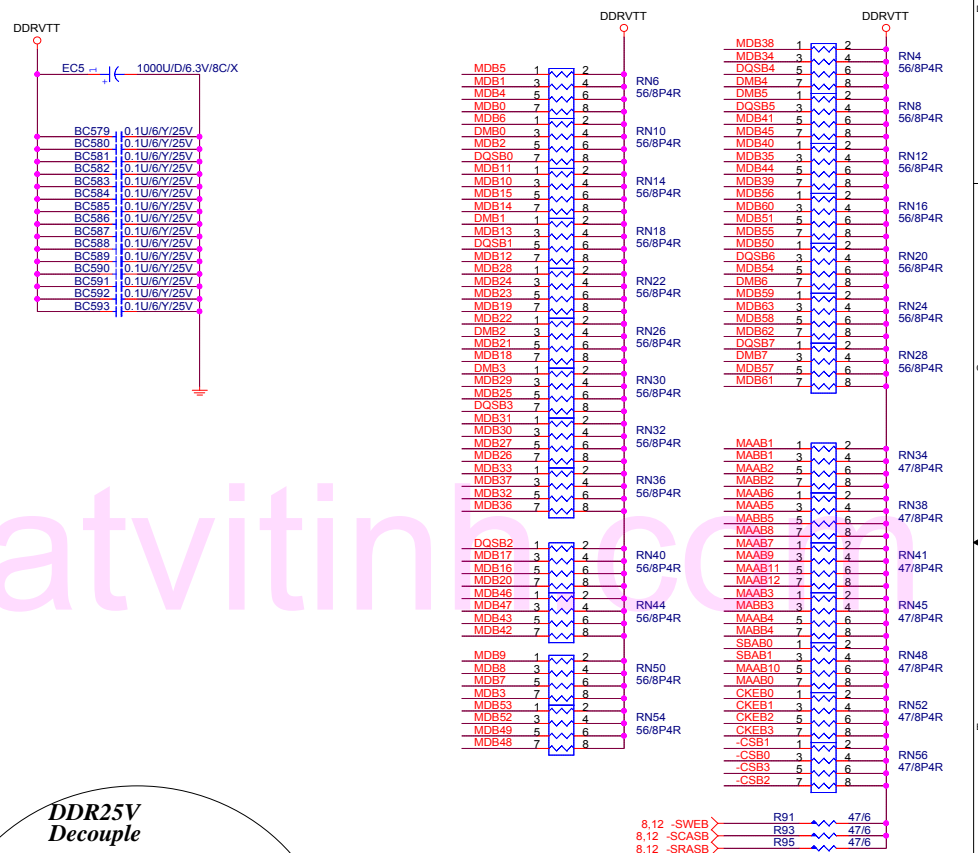




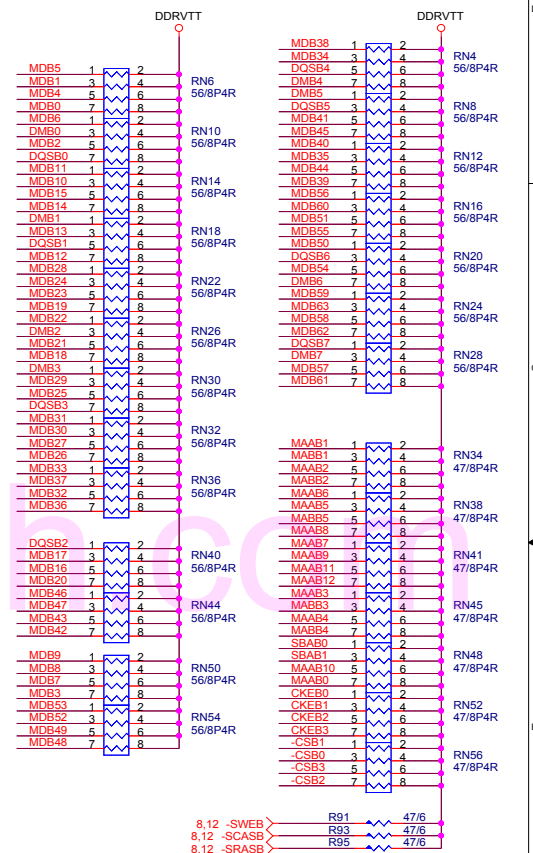




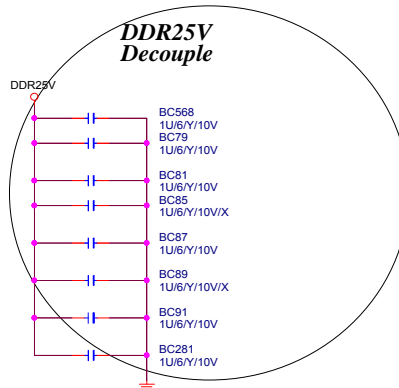
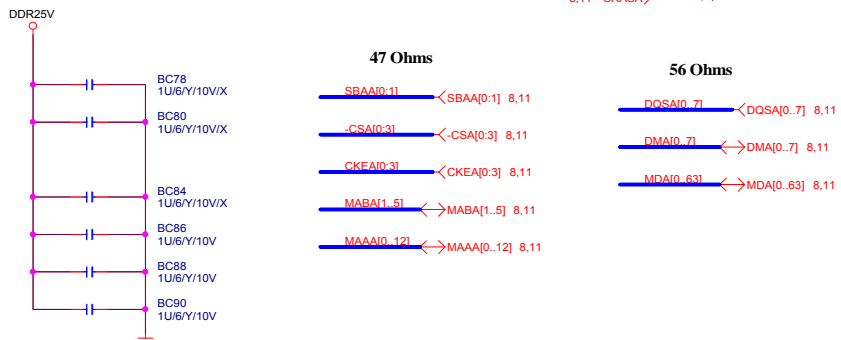
DDR TERMINATION CHANNEL A

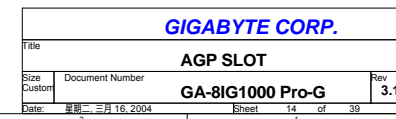


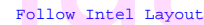
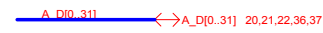
CHANNEL B



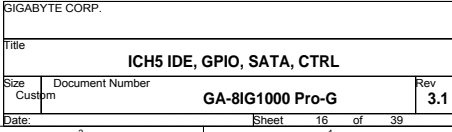
DDR25V
Decouple

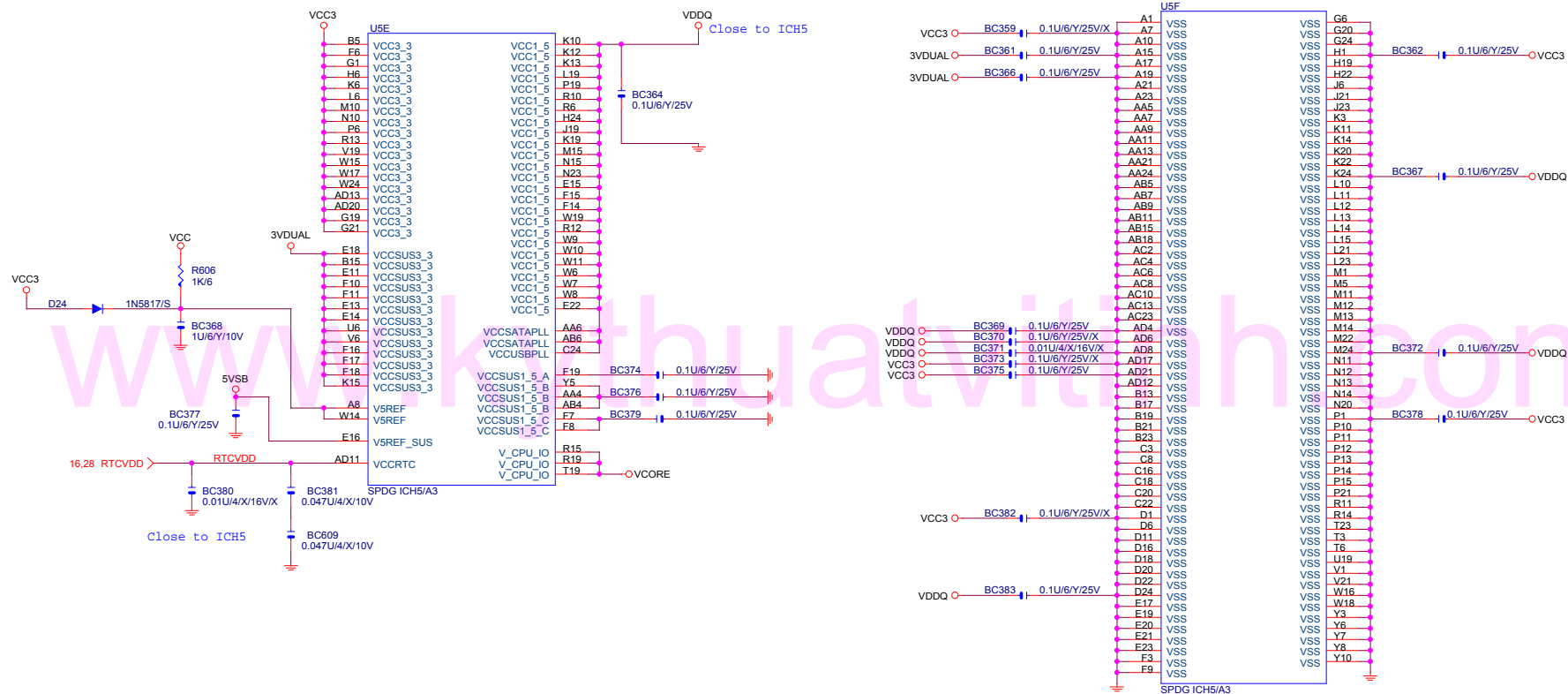


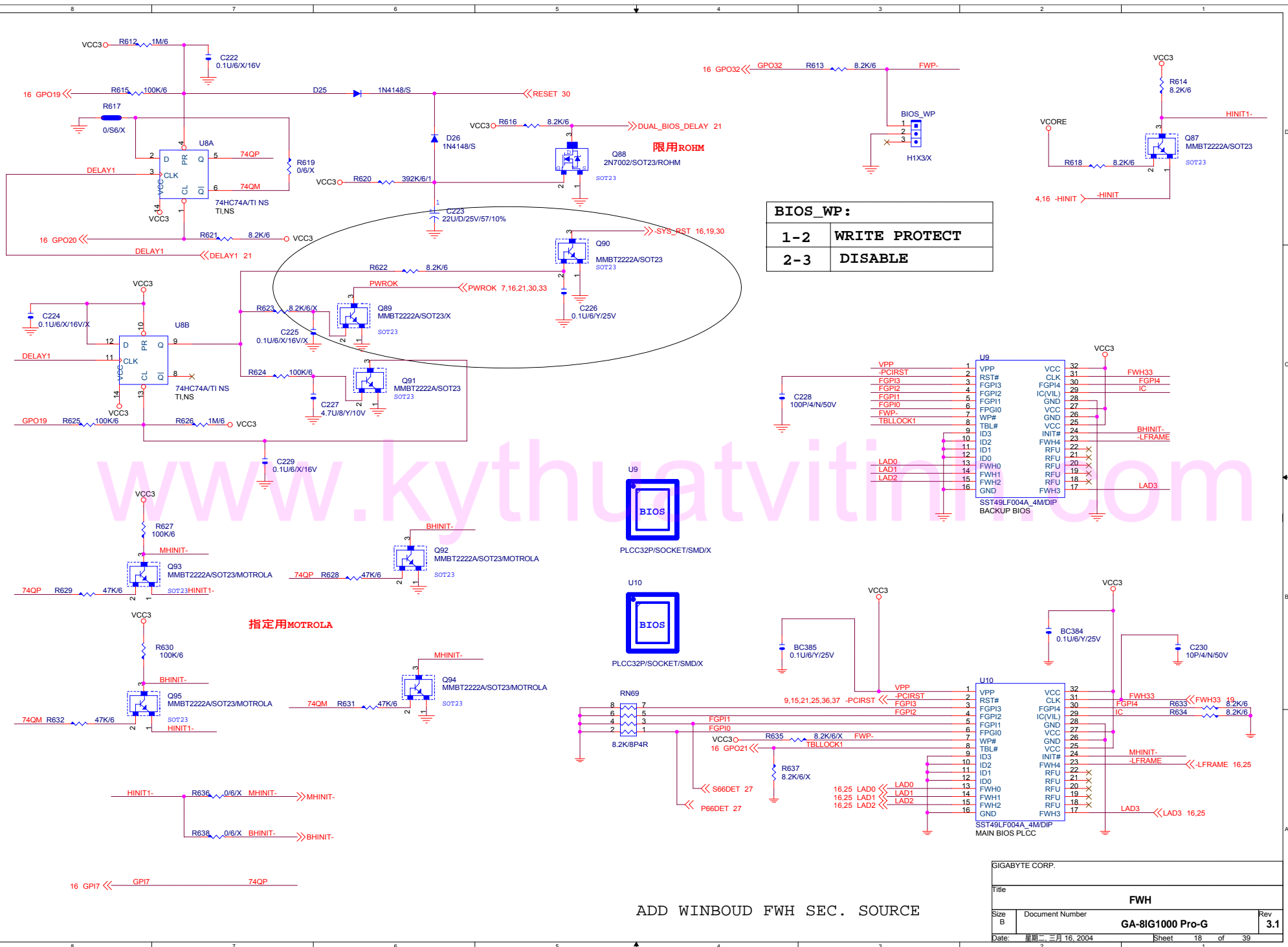


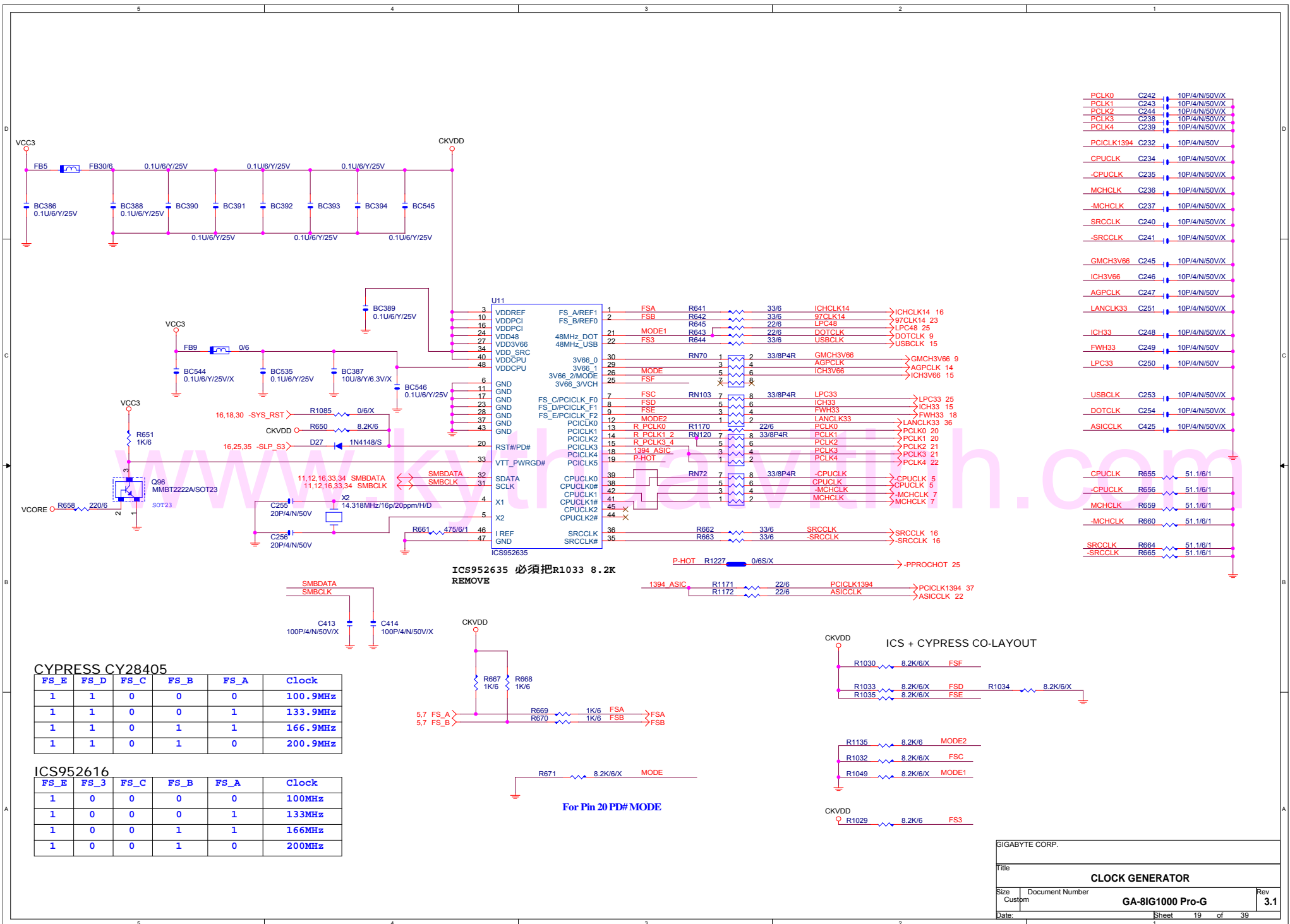


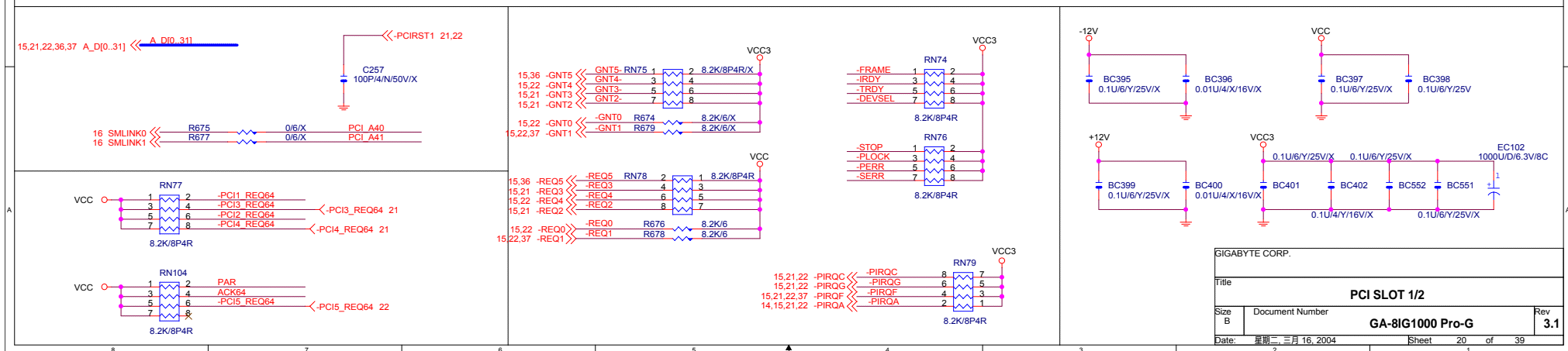
19 USBCLK > USBCLK

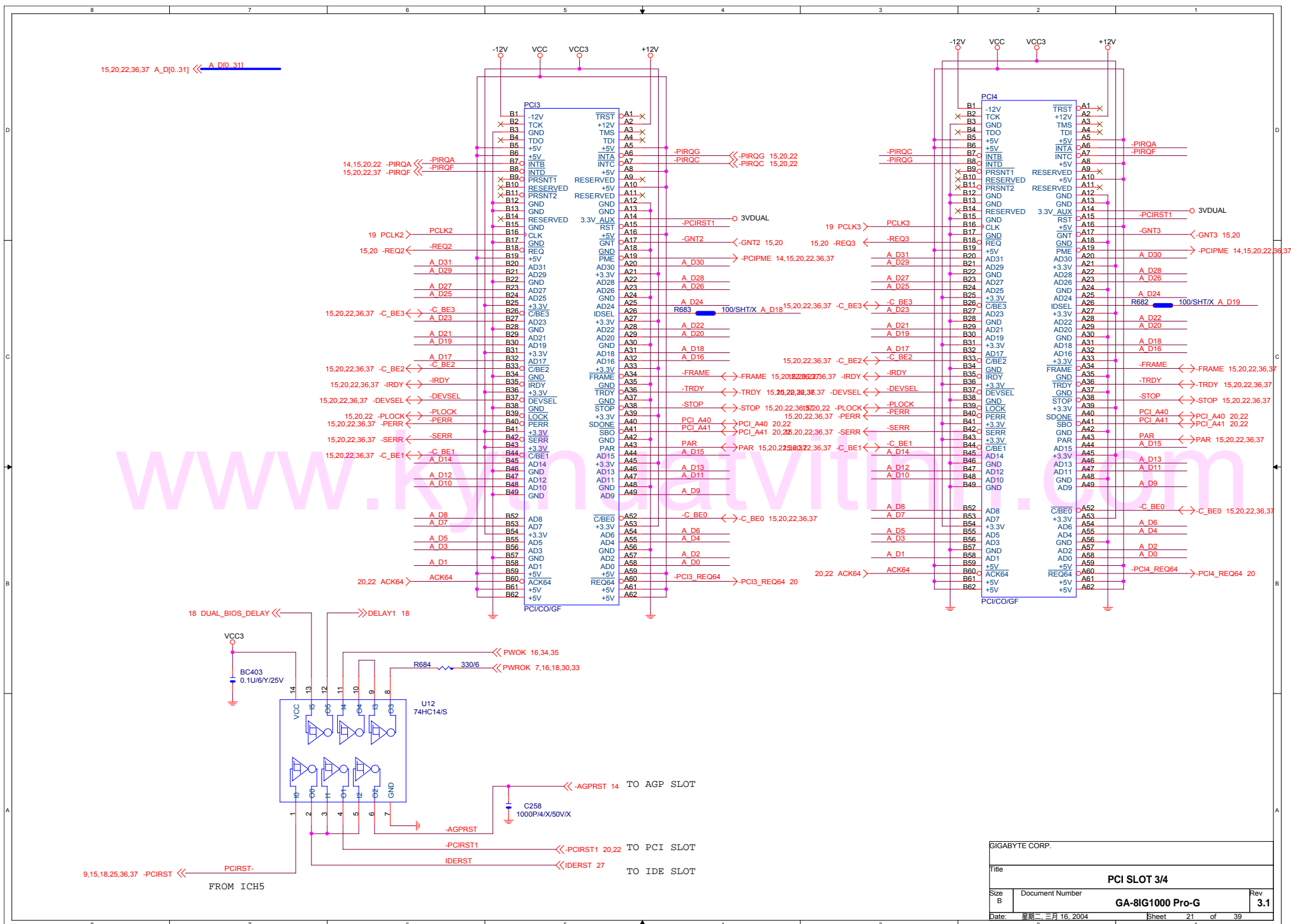






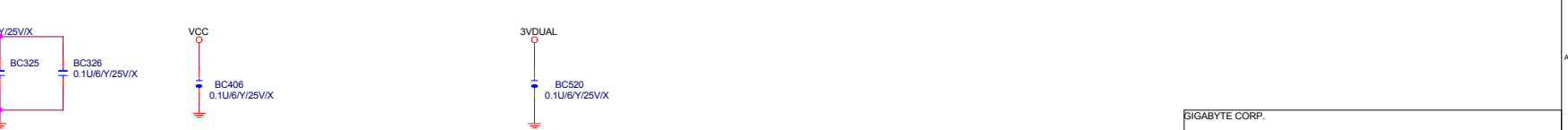
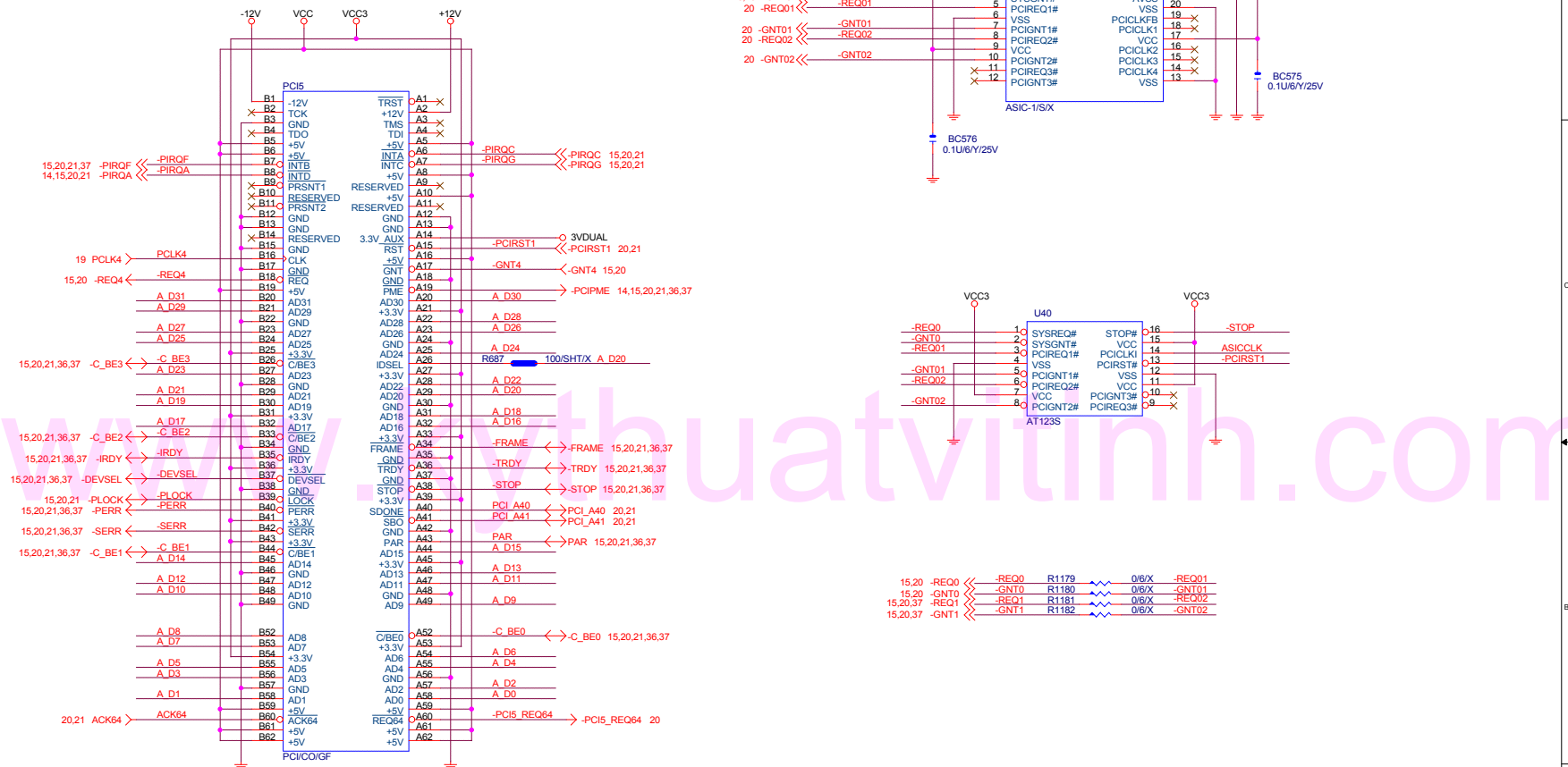






5 4 3 2 1

15,20,21,36,37 A_D[0..31] <-> A_D[0..31]



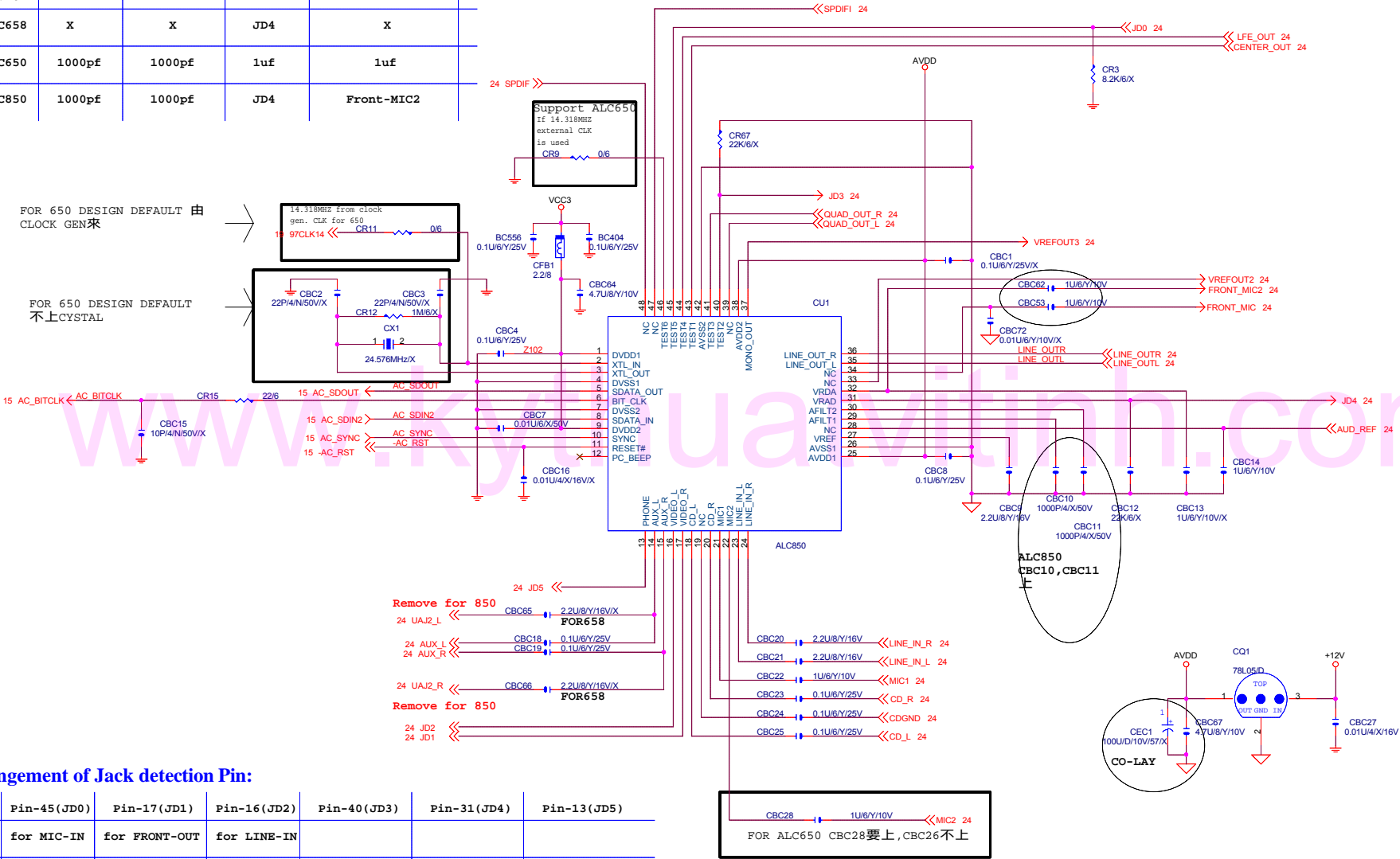
GIGABYTE CORP.			
Title			
PCI SLOT 5			
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Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

FOR 650 DESIGN DEFAULT 由
CLOCK GEN来

FOR 650 DESIGN DEFAULT
不上CRYSTAL

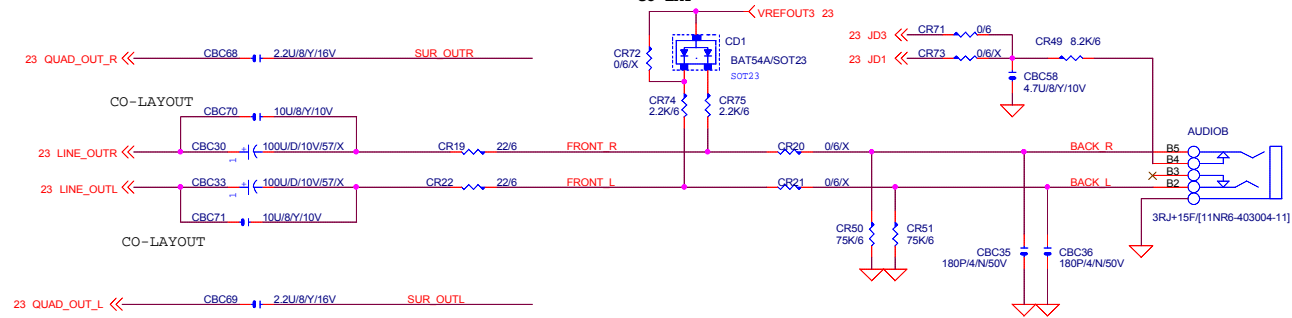


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

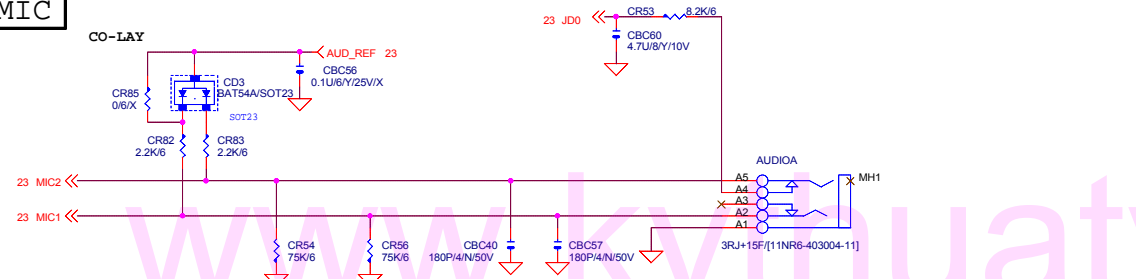
LINE OUT

JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



LINE OUT SENSING
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

MIC



MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓 與CR43,CR32 並聯求出阻抗)
7.1k ohm>R>2.3k ohm==>microphone in
R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

2x5 header for 850

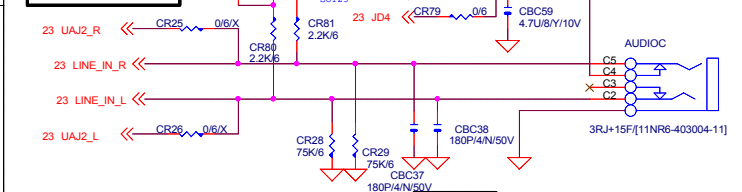
For 850 if JD5 = low AUX-In is configured as input
For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

For 850 AUX-In is shared to Surr-Back out

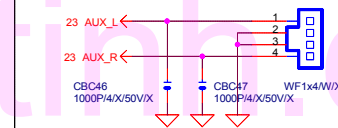
LINE IN SENSING(當OUTPUT)
R>4K OHM=>POWER SPEAKER
4K OHM>R>400 OHM=>MICROPHONE
R<400 OHM=>HEADPHONE

LINE IN SENSING(當INPUT)
swing of input signal>-40dbv(10mv)==>line in device active
swing of input signal<-40dbv(10mv)==>unknown line in device

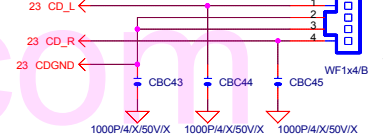
LINE-IN



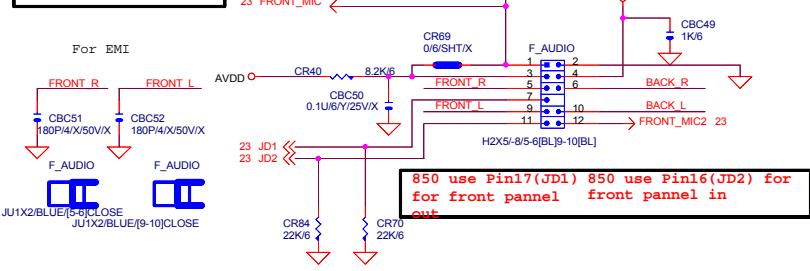
AUX IN DEFAULT NO POP



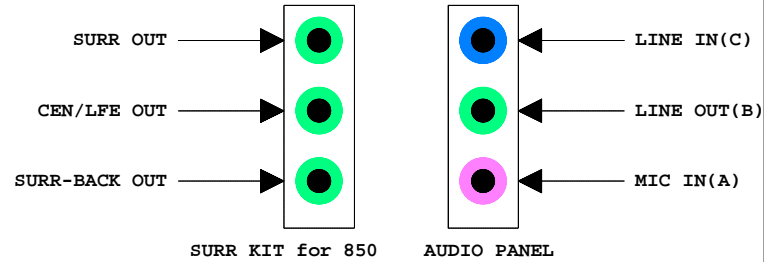
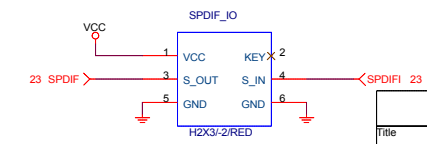
CD IN

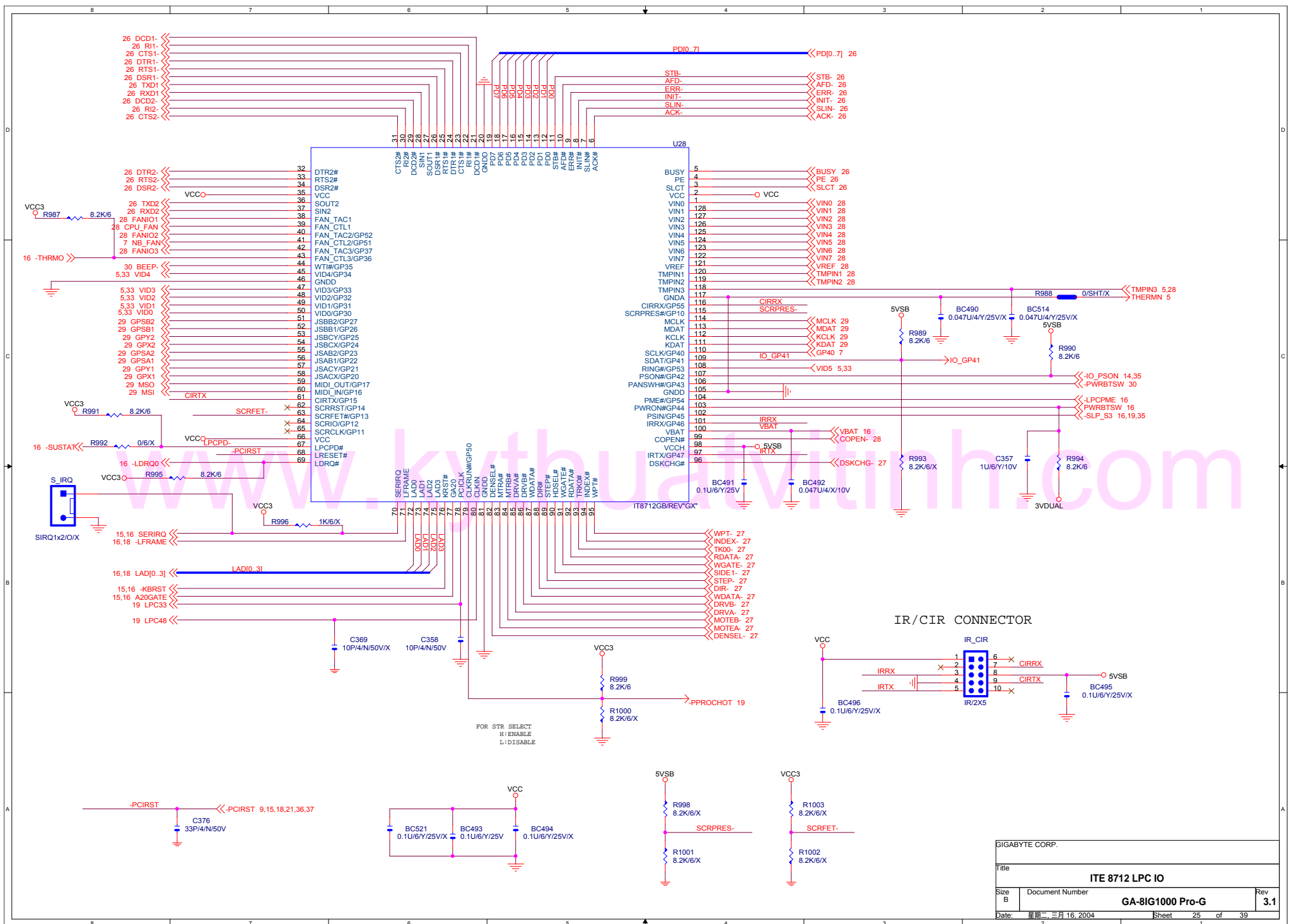


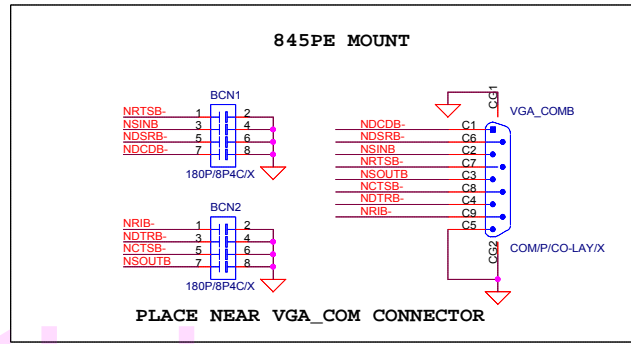
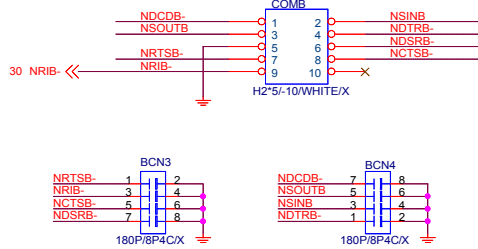
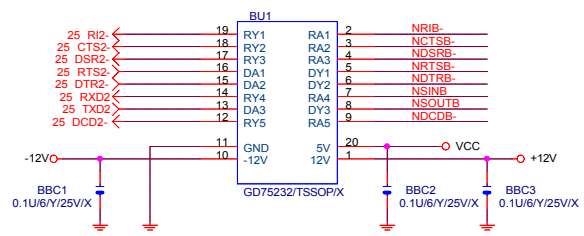
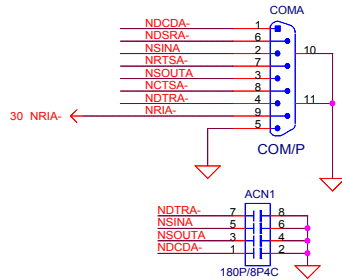
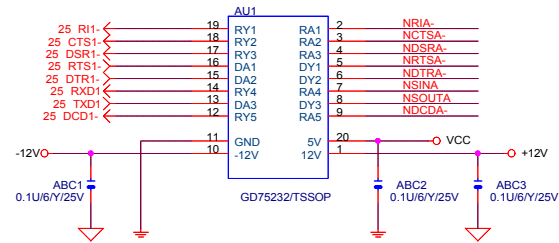
INTEL FRONT AUDIO



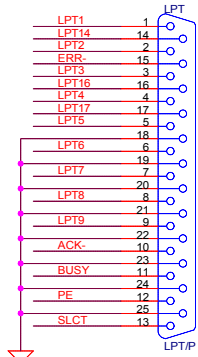
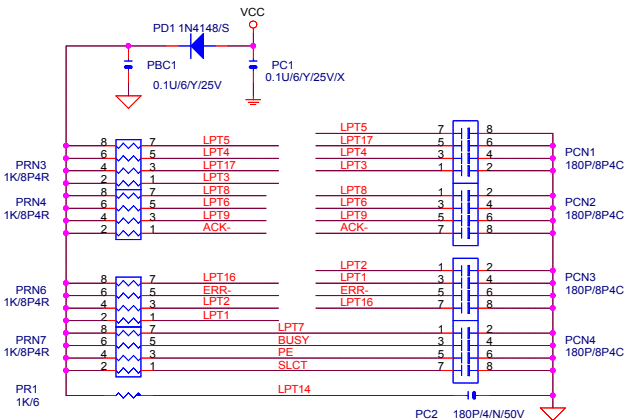
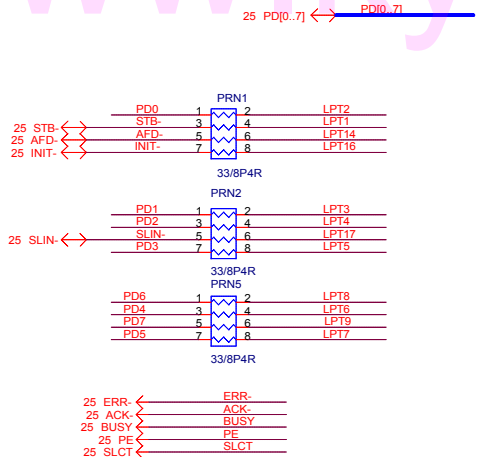
SPDIF_IO

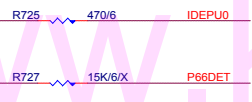
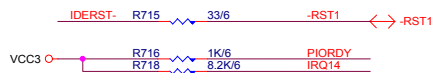
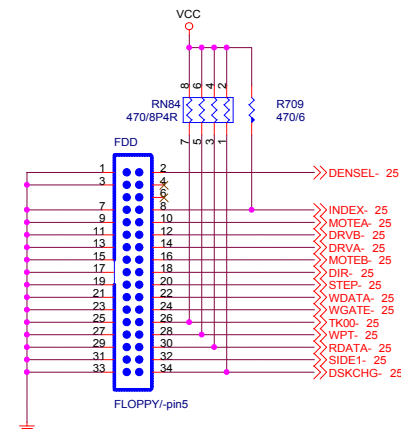
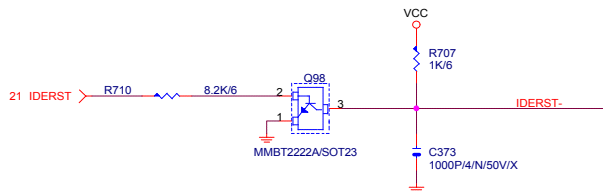






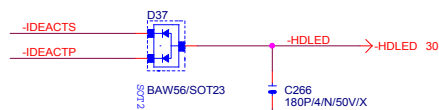
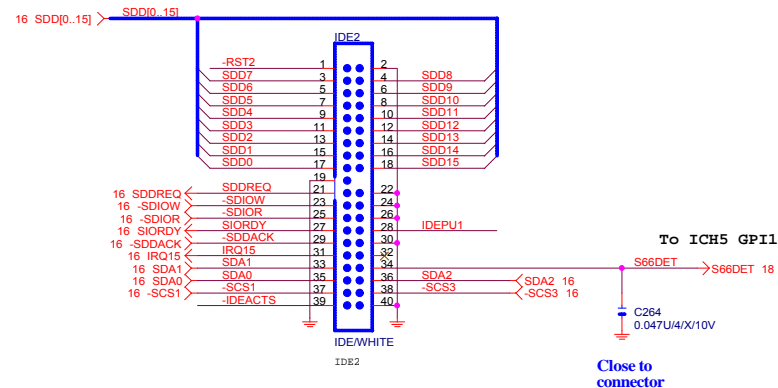
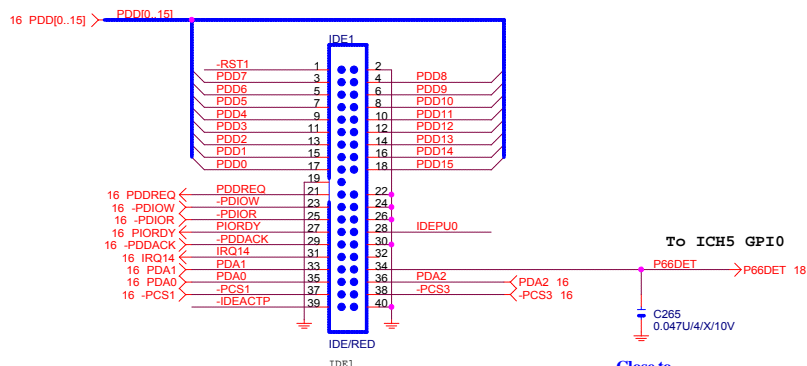
PLACE NEAR VGA_COM CONNECTOR





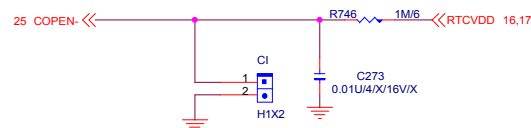
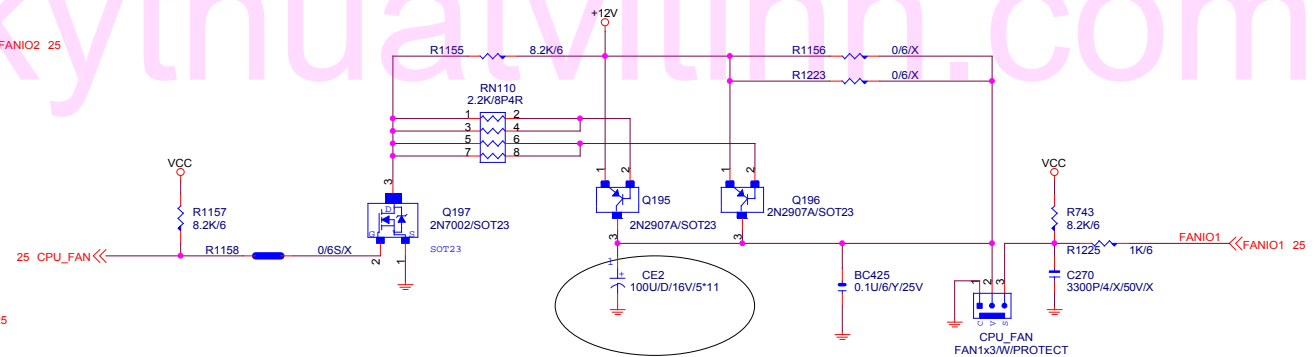
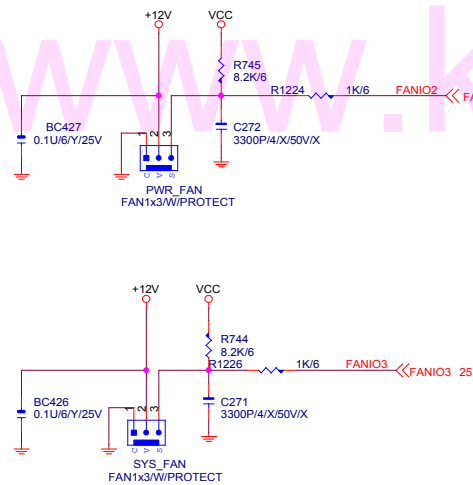
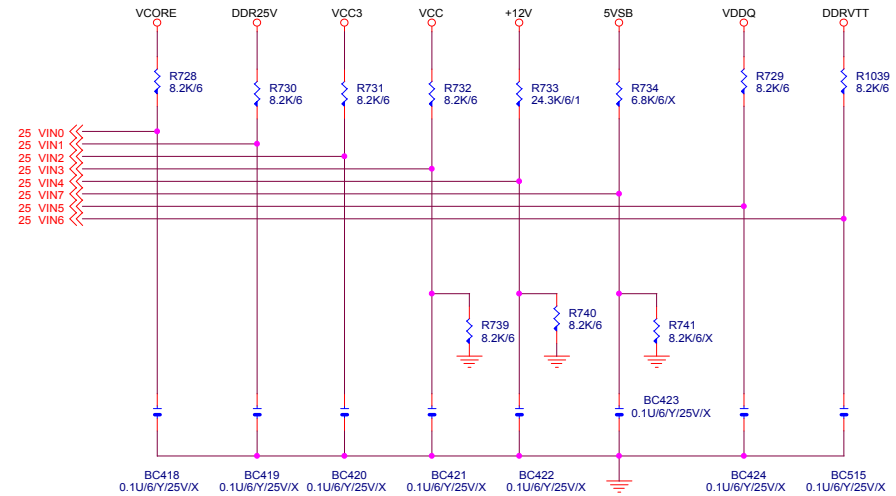
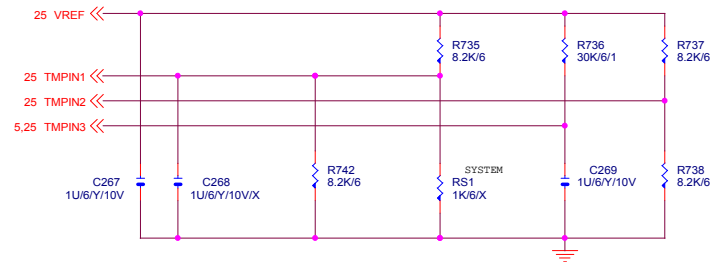
PRIMARY IDE CONNECTOR

SECONDARY IDE CONNECTOR



GIGABYTE CORP.			
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IDE CONNECTOR			
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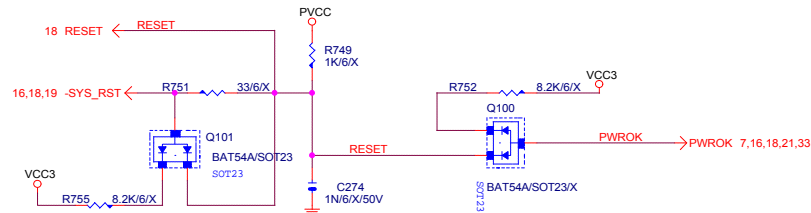
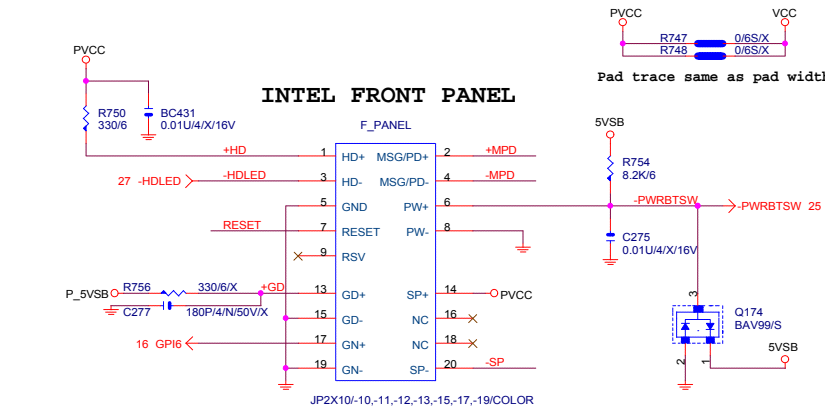
Hardware Monitor circuits



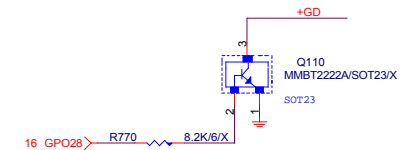
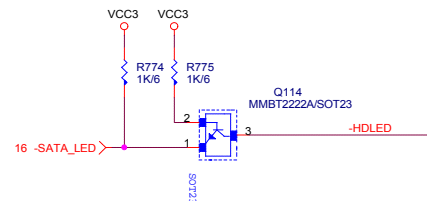
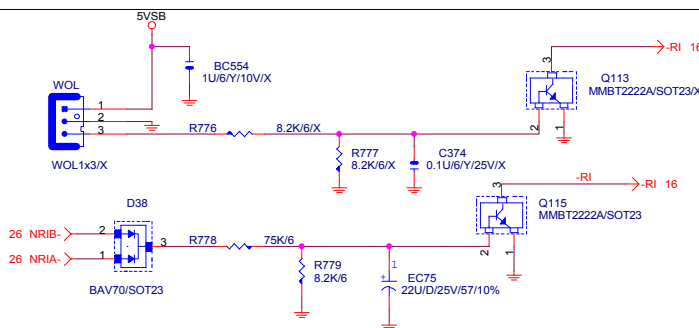
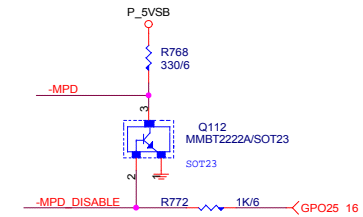
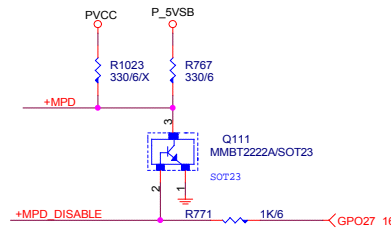
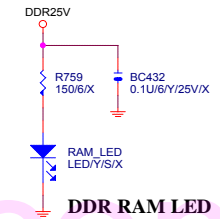
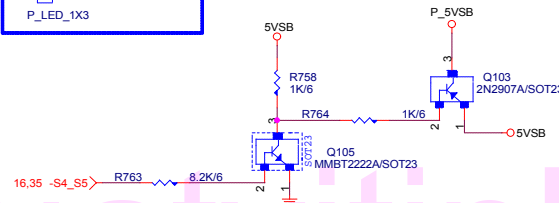
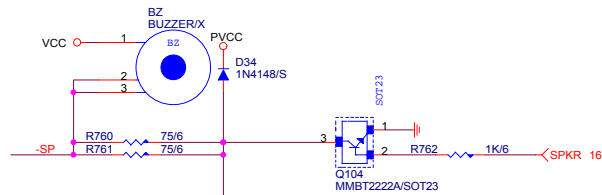
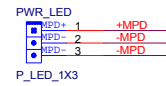


GIGABYTE CORP.				
Title				
KB & PS2 MOUSE & IR				
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INTEL FRONT PANEL

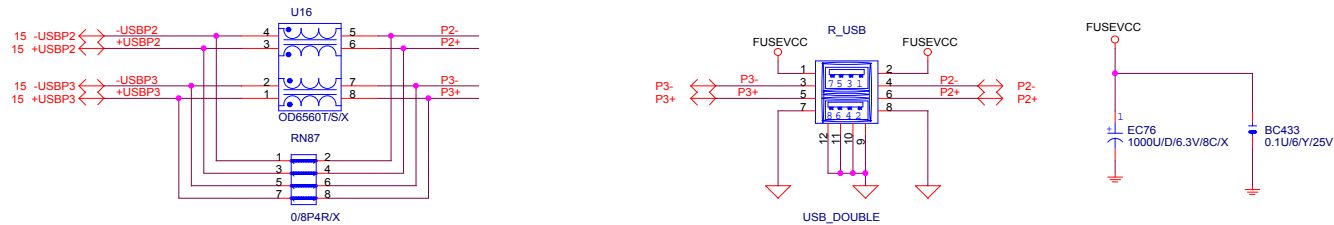


3 PIN POWER LED

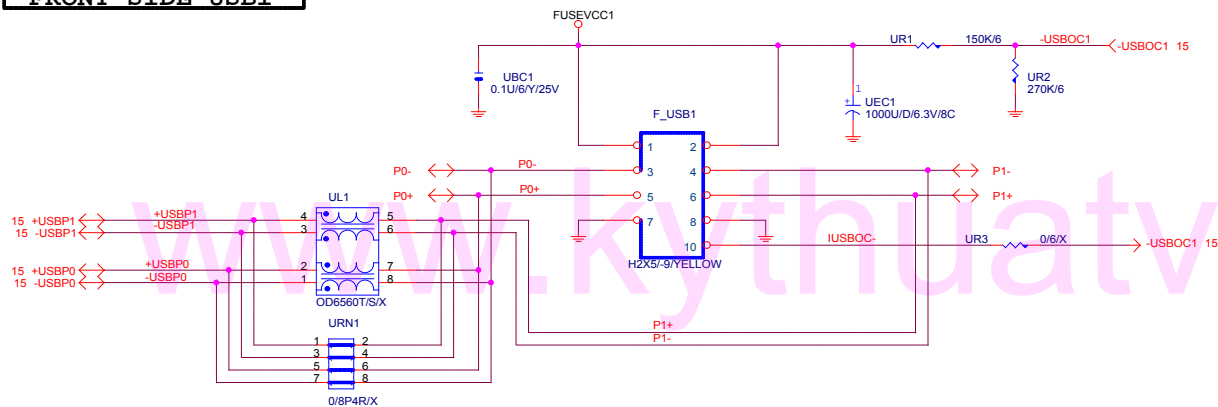


GIGABYTE CORP.			
Title			
PANEL & STR LED & RI			
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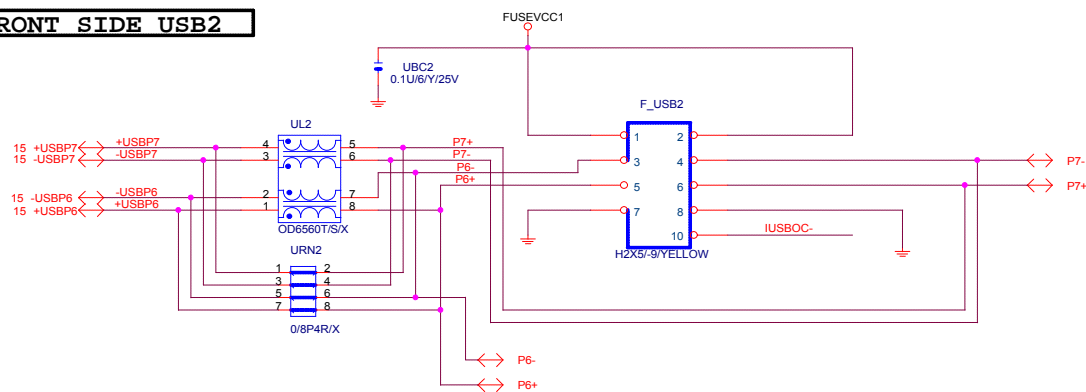
REAR USB



FRONT SIDE USB1

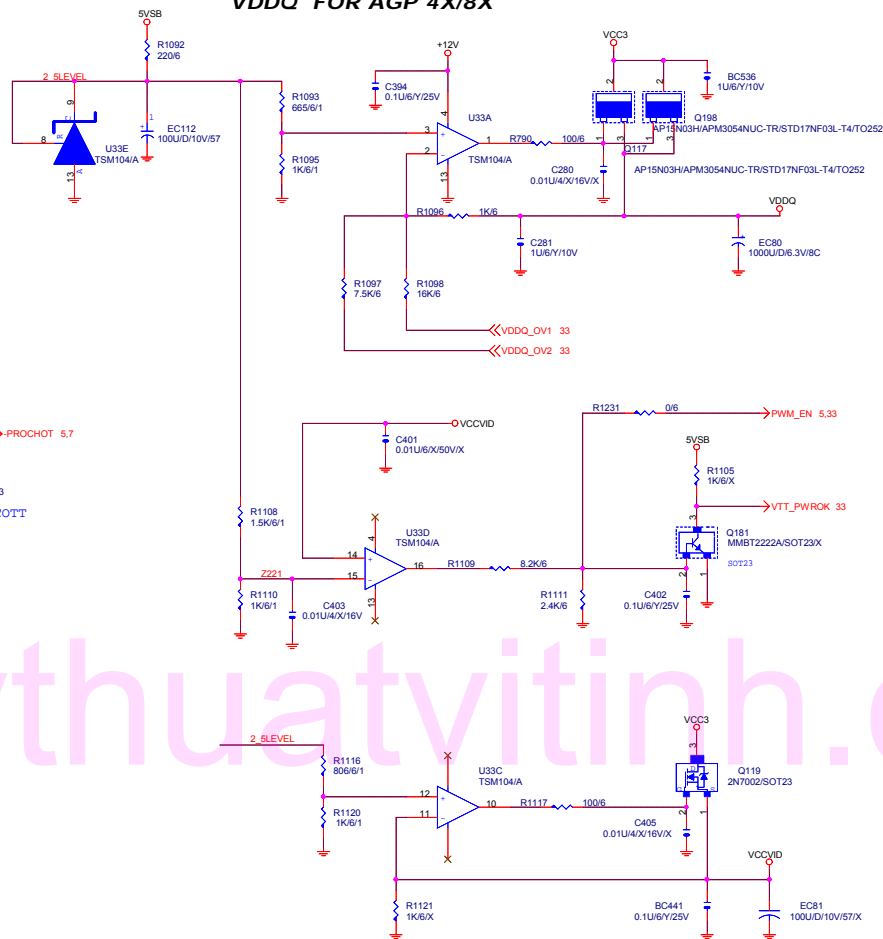
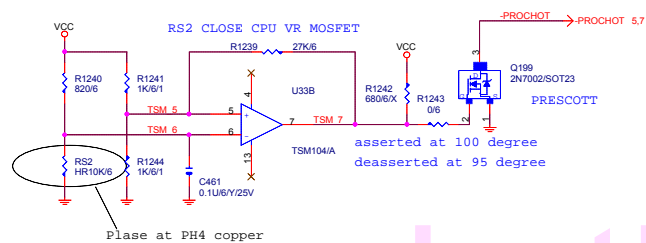


FRONT SIDE USB2

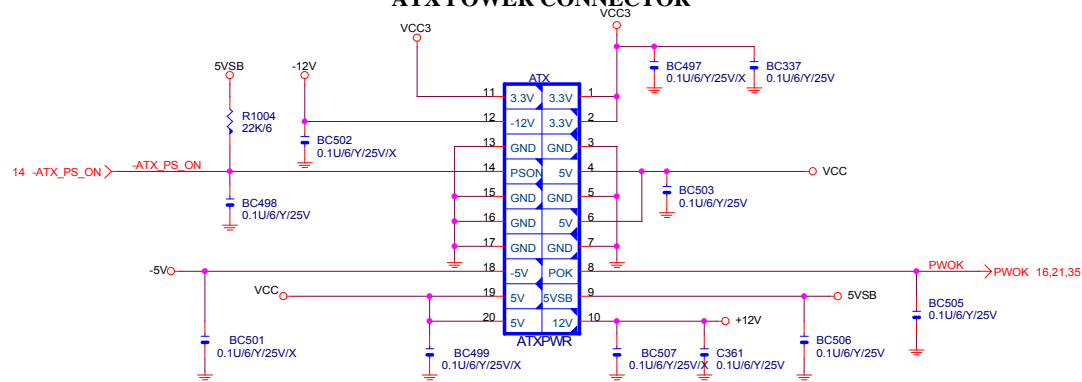


DDR25V FOR DDR DIMM & NB

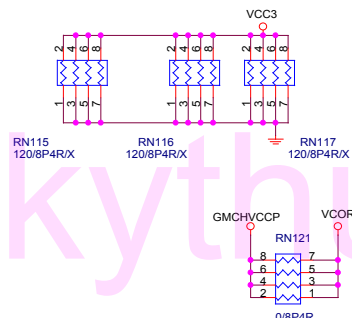
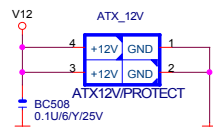
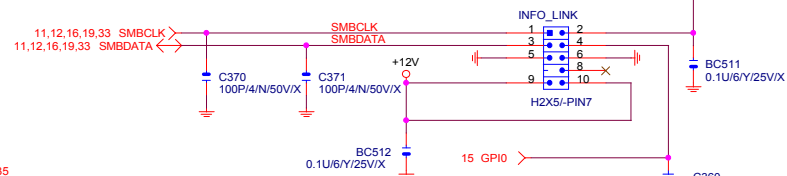
VDDQ FOR AGP 4X/8X



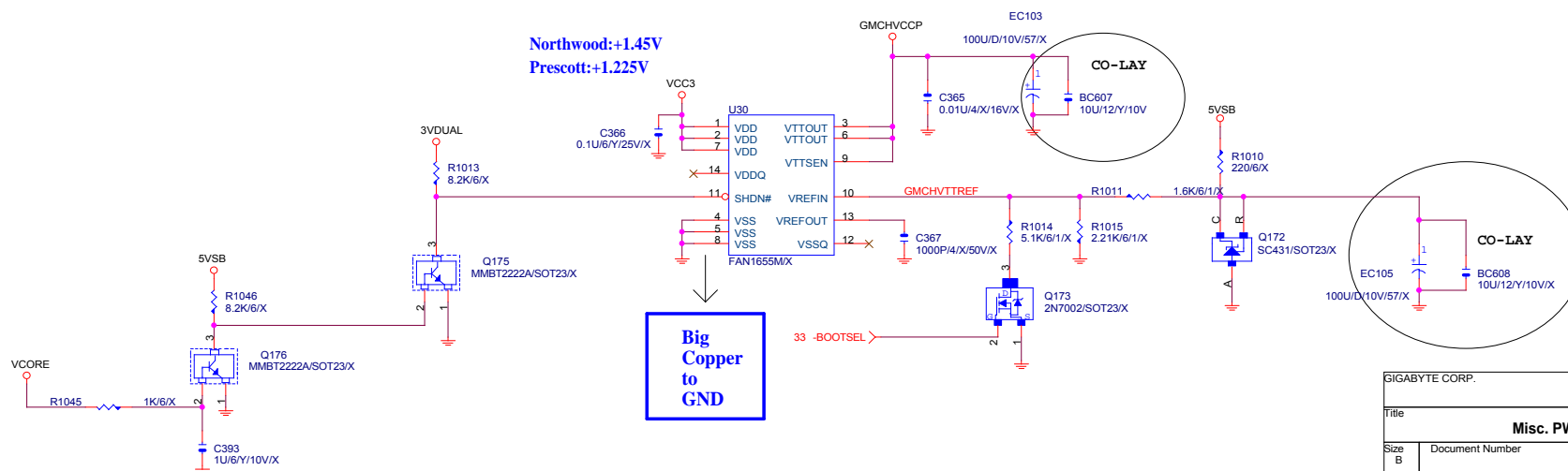
ATX POWER CONNECTOR



SMBUS CONN.



Northwood:+1.45V
Prescott:+1.225V



Big Copper
to
GND

GIGABYTE CORP.			
Title Misc. PWR & ATX CONN.			
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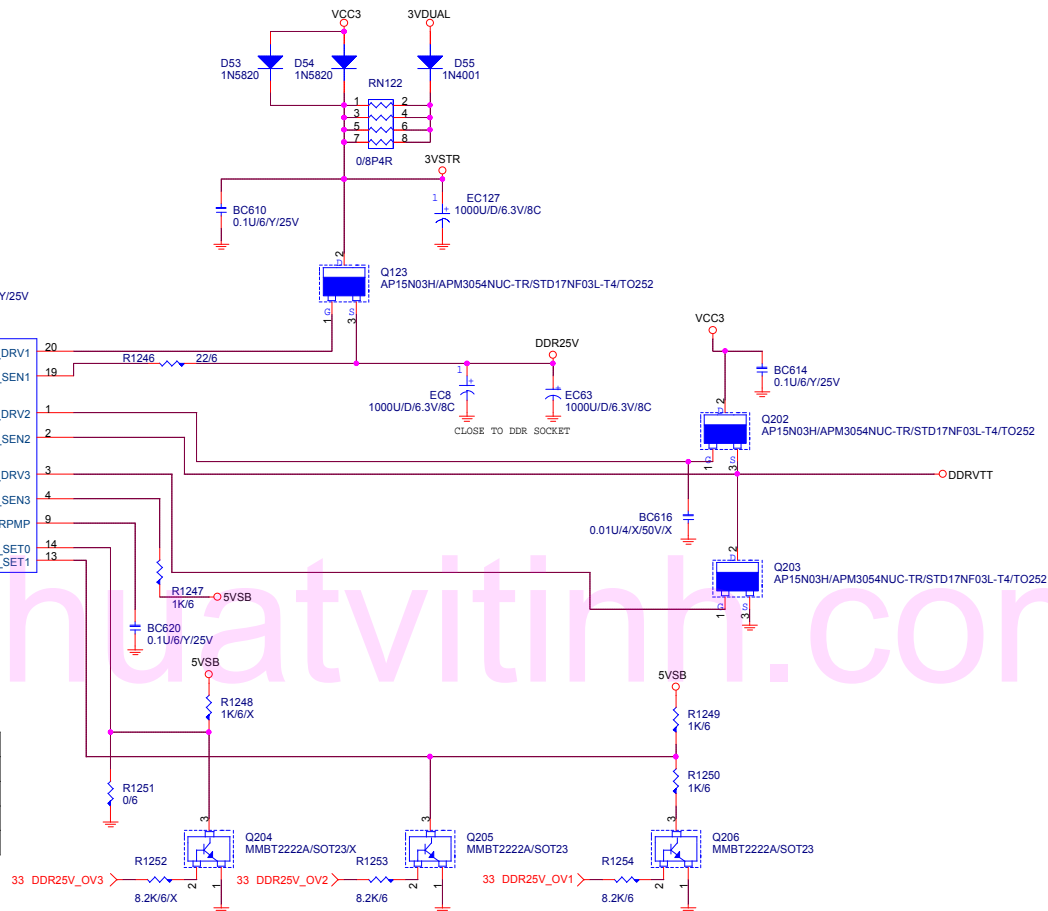
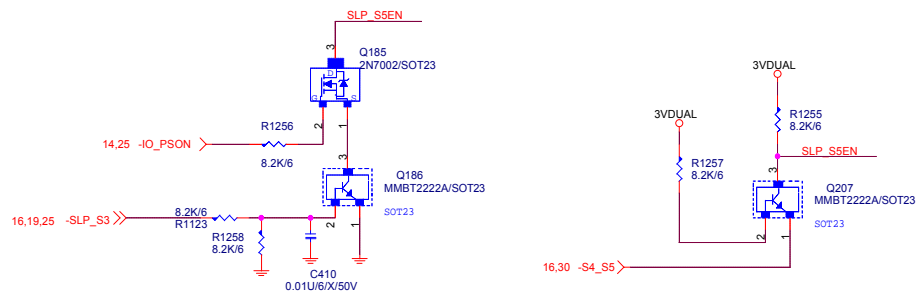
1.25V VTT_DDR LINEAR SOLUTION

DDR25_OV1,DDR25_OV2,DDR25_OV3 RESUME WELL DEFAULT HIGH

	DDR25_OV2	DDR25_OV1	DDR25_OV3	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V
2.8V	HIGH	HIGH	LOW	2.5V	0V

FOR 2.8V BIOS PROGRAMMING

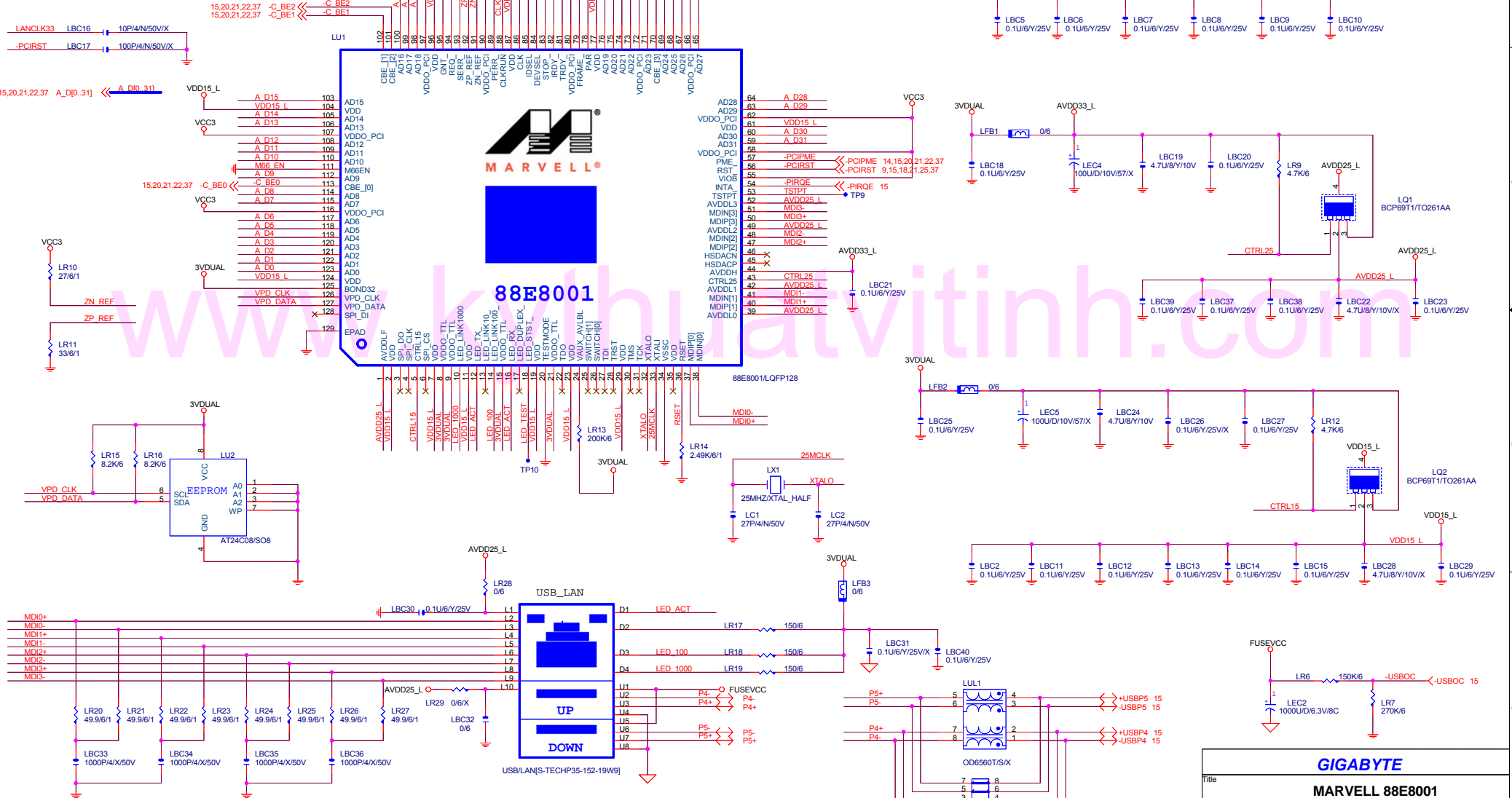
時須先PROGRAMMING 2.5V後再PROGRAMMING 2.8V

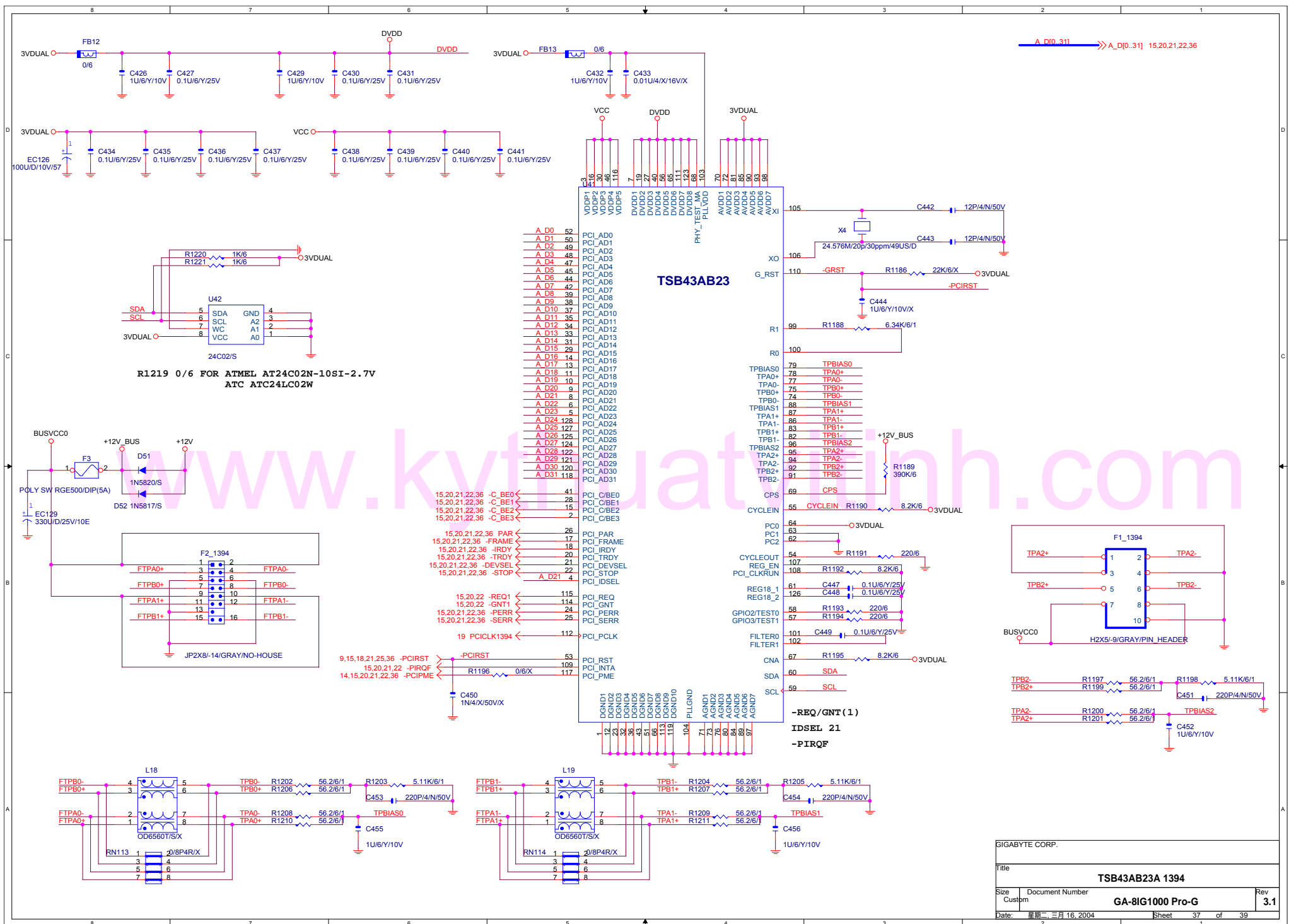


GIGABYTE THCHNOLOGIES , INC.

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- # Layout Check 注意事項
1. LU1 PIN129 需下內層GND, 至少打 22 VIA
 2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
 3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
 4. MDI正負0~3, TRACE 8:7:8, 每對之間保持 40mil





GIGABYTE GA-8IG1000 Pro-G PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT	
PCI SLOT1	16	C,F,G,A	PCLK0	-REQ01	-GNT01	
PCI SLOT2	17	F,G,A,C	PCLK1	-REQ02	-GNT02	
PCI SLOT3	18	G,A,C,F	PCLK2	-REQ2	-GNT2	
PCI SLOT4	19	A,C,F,G	PCLK3	-REQ3	-GNT3	
PCI SLOT5	20	C,F,G,A	PCLK4	-REQ4	-GNT4	
TI 1394	21	F	PCICLK1394	-REQ1	-GNT1	
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)	

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GIGABYTE GA-8IG1000 Pro-G GPIO LIST

SHEET

TITLE

GPIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL,-SMBALERT.
GPI12	I	PULL 8.2K TO VCC3,M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3,PANEL S3 POWER LED.

SHEET

TITLE

GPIP	I/O	FUNCTION
GPO23	NA	PULL 8.2K TO VCC3
GPO24	O	INTEL LAN ENABLE/DISABLE.
GPO25	O	FRONT PANEL -MPD.
GPO27	O	FRONT PANEL +MPD.
GPO28	O	GREEN LED
GPO32	O	BIOS WRITE PROTECT.
GPO33	O	SATA LED.
GPO34	I	CLEAR PASSWORD.

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